REMARKS

In the Restriction Requirement dated December 23, 2005, the Examiner requests that Applicant elect one of the following groups for prosecution on the merits:

Group I - Claims 20-37, drawn to a method of fabricating a semiconductor memory element arrangement; and

Group II - Claim 38, drawn to a semiconductor memory element arrangement.

Applicant hereby elects Group I (claims 20-37) with traverse.

The relevant statutory and regulatory provisions, 35 USC 121 and 37 CFR 1.142, require for a restriction requirement that there be "two or more independent ***and*** distinct inventions" (emphasis added). That is, there is an additional requirement of also being "independent" for restriction.

Below is a comparison between the features of the independent method claim 20 and the independent product claim 38. The main differences are shown in bold italic.

20. A method for fabricating a semiconductor memory element arrangement, comprising the steps of:	38. A semiconductor memory element arrangement, in which a plurality of semiconductor memory elements are arranged in a matrix-like manner in a plurality of rows and columns, each semiconductor memory element comprising:
forming a first electrically insulating layer on a substrate;	an electrically insulating layer formed on a substrate;
forming a layer system, including a floating gate and a multiple tunnel barrier arrangement formed on the floating gate, on the ***first***	a layer system formed on the electrically insulating layer, wherein the layer system includes a floating gate and a tunnel barrier

electrically insulating layer;	arrangement formed on the floating gate ***and forming a multiple tunnel barrier***;
forming a first trench structure in the layer system, the first trench structure having first trenches arranged parallel to one another and extending as far as the ***first*** electrically insulating layer;	a first trench structure formed in the layer system and having first trenches arranged parallel to one another and extending as far as the electrically insulating layer;
forming a second trench structure in the layer system, the second trench structure having second trenches arranged parallel to one another and extending as far as the ***first*** electrically insulating layer, the second trenches being arranged perpendicular to the first trenches;	a second trench structure formed in the layer system and having second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the electrically insulating layer;
forming, in the first and second trench structures, a first gate electrode adjacent to the floating gate through which first gate ***electrode electrical charge can be fed or can be dissipated from***; and	a first gate electrode formed in the first and second trench structures and adjacent to the floating gate, wherein the first gate ***electrode determines the charge carriers stored in the floating gate***; and
forming, in the first and second trench structures, a second gate electrode adjacent to the tunnel barrier arrangement, wherein through the second gate electrode an ***electrical*** charge transmission of the ***multiple*** tunnel barrier arrangement can be controlled.	a second gate electrode formed in the first and second trench structures and adjacent to the tunnel barrier arrangement, wherein via the second gate electrode the charge transmission of the tunnel barrier arrangement may be controlled.

Reconsideration and withdrawal of this Restriction Requirement is terefore respectfully requested.

Further, if possible, Applicant respectfully requests the Examiner to wait to make the Restriction Requirement final until any action after the next Office Action.

An action on the merits of all the elected claims and a Notice of Allowance thereof are respectfully requested.

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Respectfully submitted,

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